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Bertness

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(54) **ELECTRONIC BATTERY TESTER**

(75) Inventor: **Kevin I. Bertness**, Batavia, IL (US)

(73) Assignee: **Midtronics, Inc.**, Willowbrook, IL (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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(51) **Int. Cl.**[7] **G01N 27/416**; H01M 10/48
(52) **U.S. Cl.** **324/430**; 324/427; 320/161
(58) **Field of Search** 324/427, 430, 324/433; 340/636; 320/151, 156, 161

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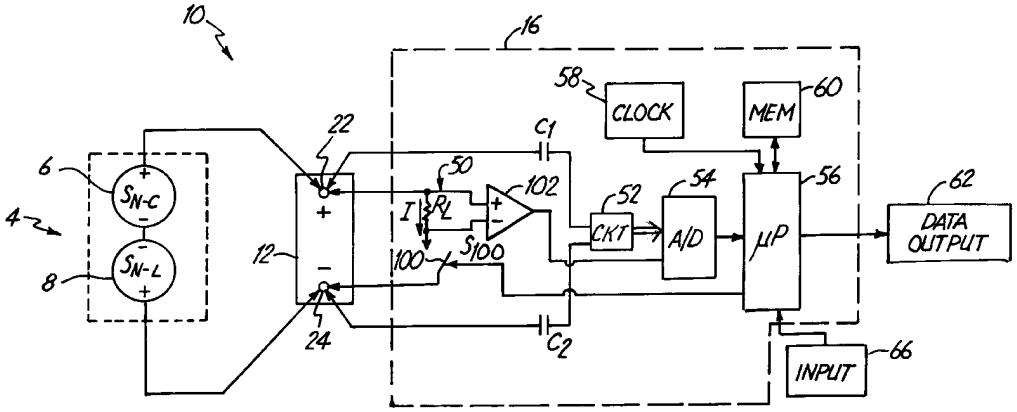
Primary Examiner—Glenn W. Brown
Assistant Examiner—Vincent Q. Nguyen
(74) *Attorney, Agent, or Firm*—Westman, Champlin & Kelly, P.A.

(57) **ABSTRACT**

A microprocessor couples to a voltage sensor through an analog to digital converter. The voltage sensor is adapted to be coupled across terminals of a battery. A small current source is also provided and adapted to be coupled across the terminal to the battery. The current source is momentarily applied to the battery and the resulting change in voltage is monitored using the microprocessor. The microprocessor calculates battery conductance based upon the magnitude of the differential current and the change in voltage and thereby determines the condition of the battery.

14 Claims, 5 Drawing Sheets



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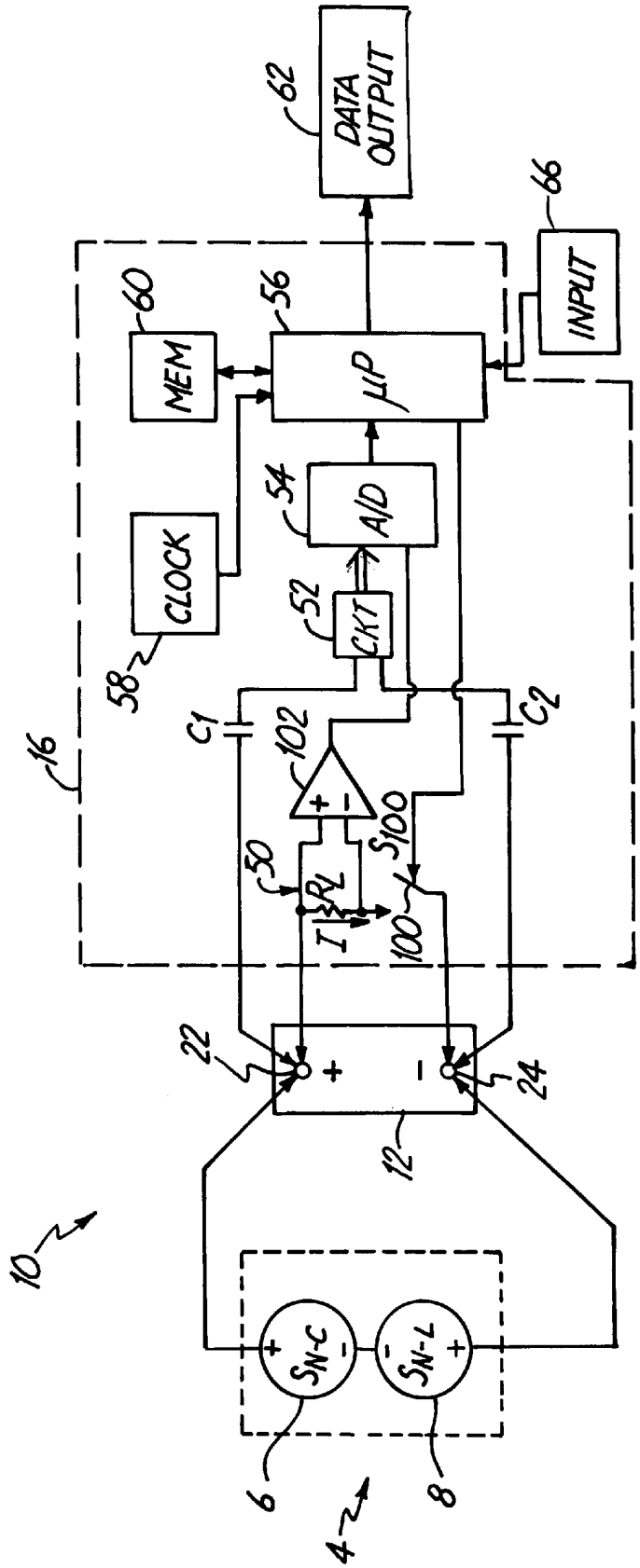
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INPUT
MEM
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μP
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A/D
CLOCK
58
52
CKT
C1
C2
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16
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S100
100
22
24
12
10
SN-C
SN-L
6
8
4

Fig. 1

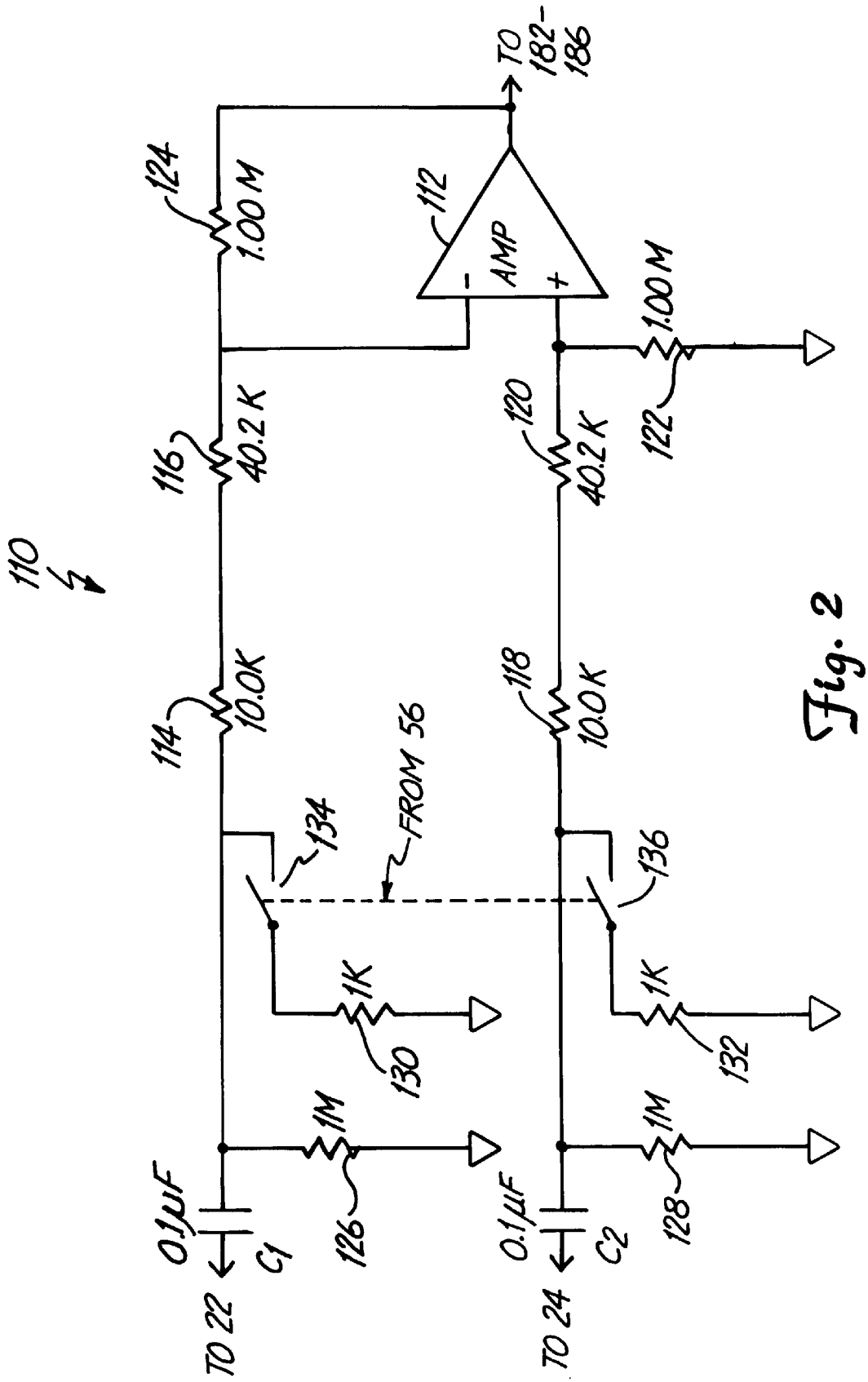
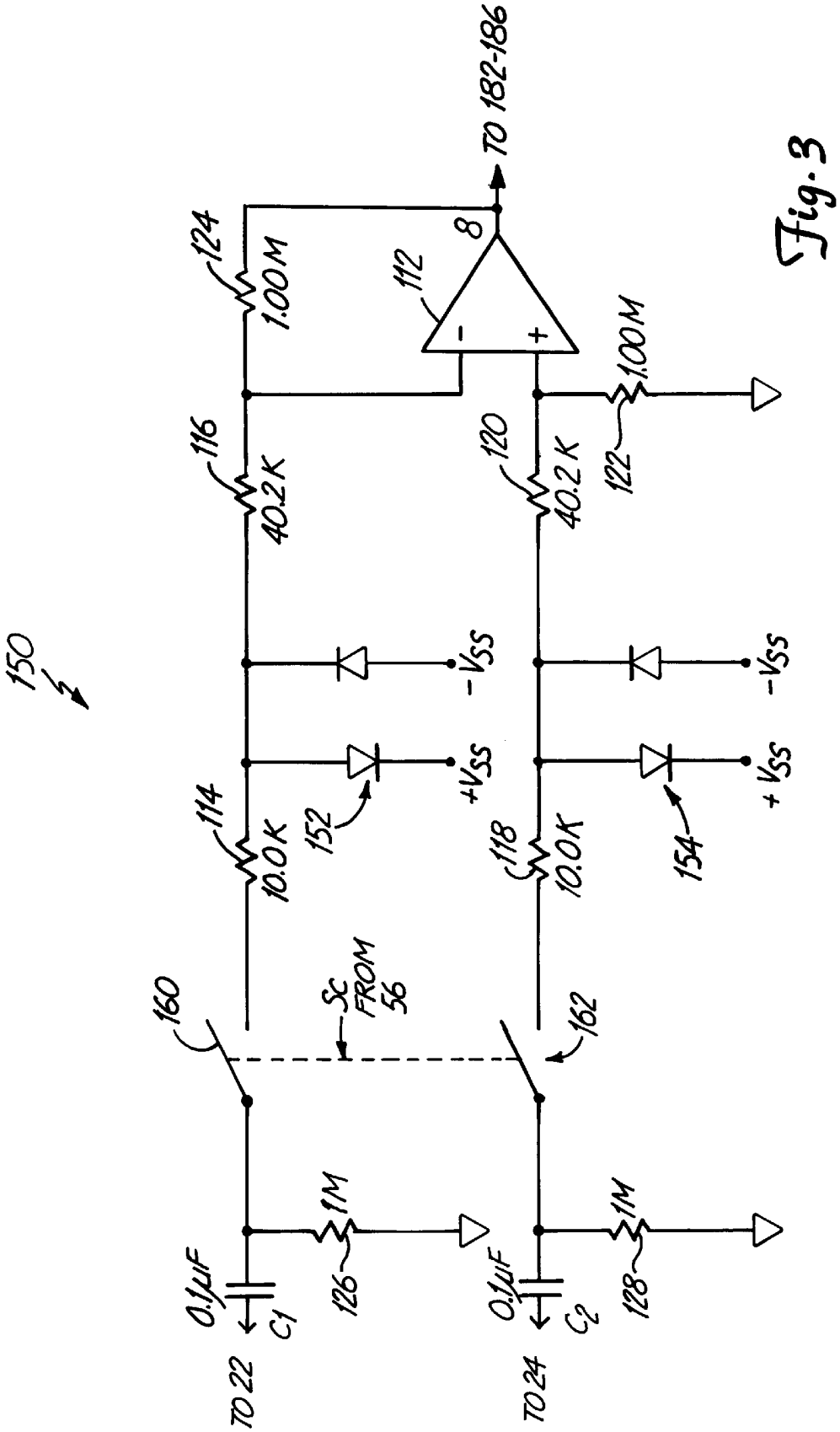

110
TO 182-186
124
1.00 M
112
AMP
-
+
1.00 M
116
40.2 K
120
40.2 K
122
114
10.0K
118
10.0K
FROM 56
134
136
1K
130
1K
132
1M
126
1M
128
0.1μF
C1
0.1μF
C2
TO 22
TO 24

Fig. 2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TO 182-186
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1.00M
112
8
116
40.2K
120
40.2K
122
1.00M
-VSS
+VSS
114
10.0K
152
118
10.0K
154
160
SC FROM 56
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C1
1M
126
0.1μF
C2
1M
128
TO 22
TO 24

Fig. 3

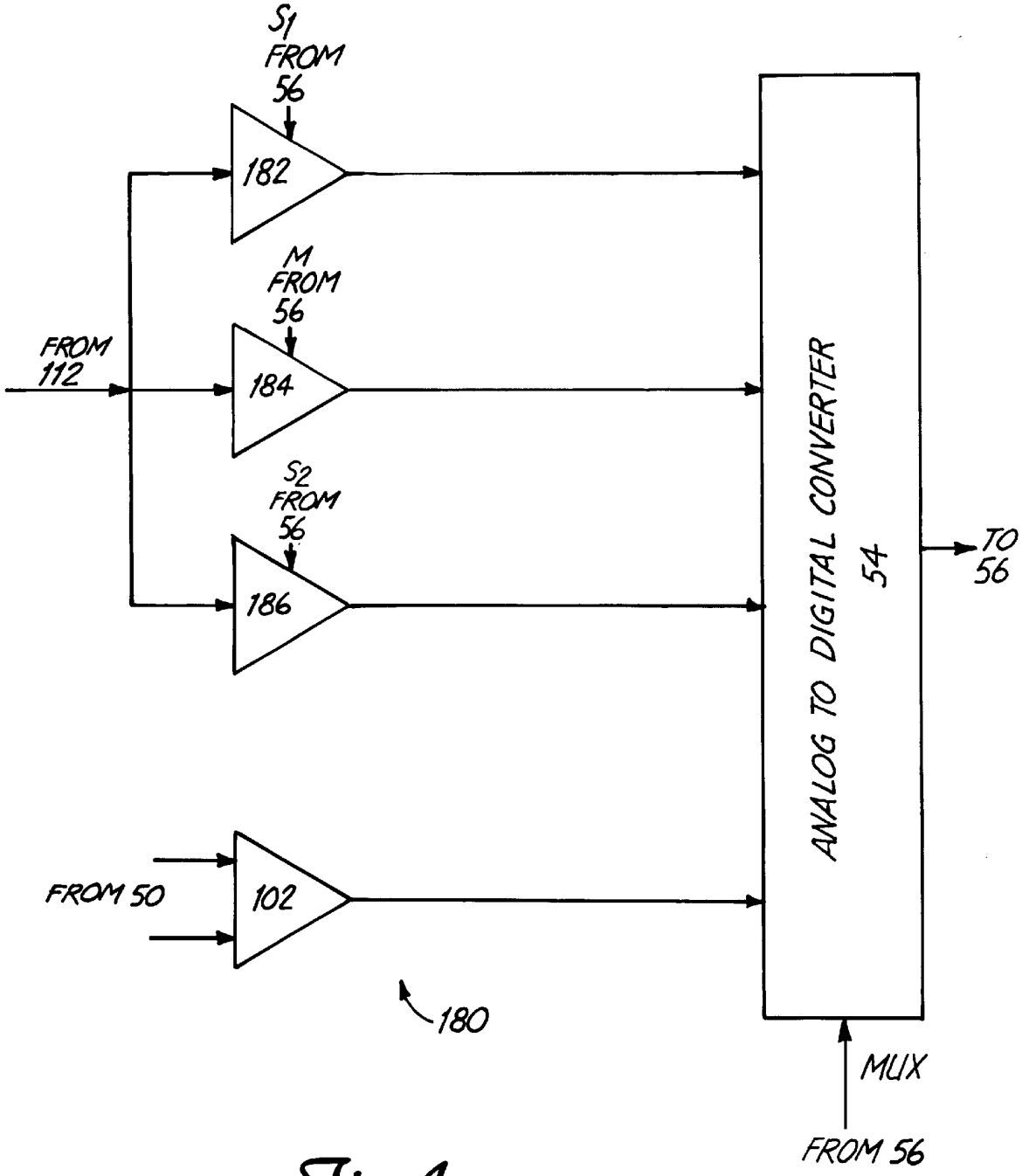
S1
FROM
56
182
M
FROM
56
FROM
112
184
S2
FROM
56
186
ANALOG TO DIGITAL CONVERTER
54
TO
56
FROM 50
102
180
MUX
FROM 56

Fig. 4

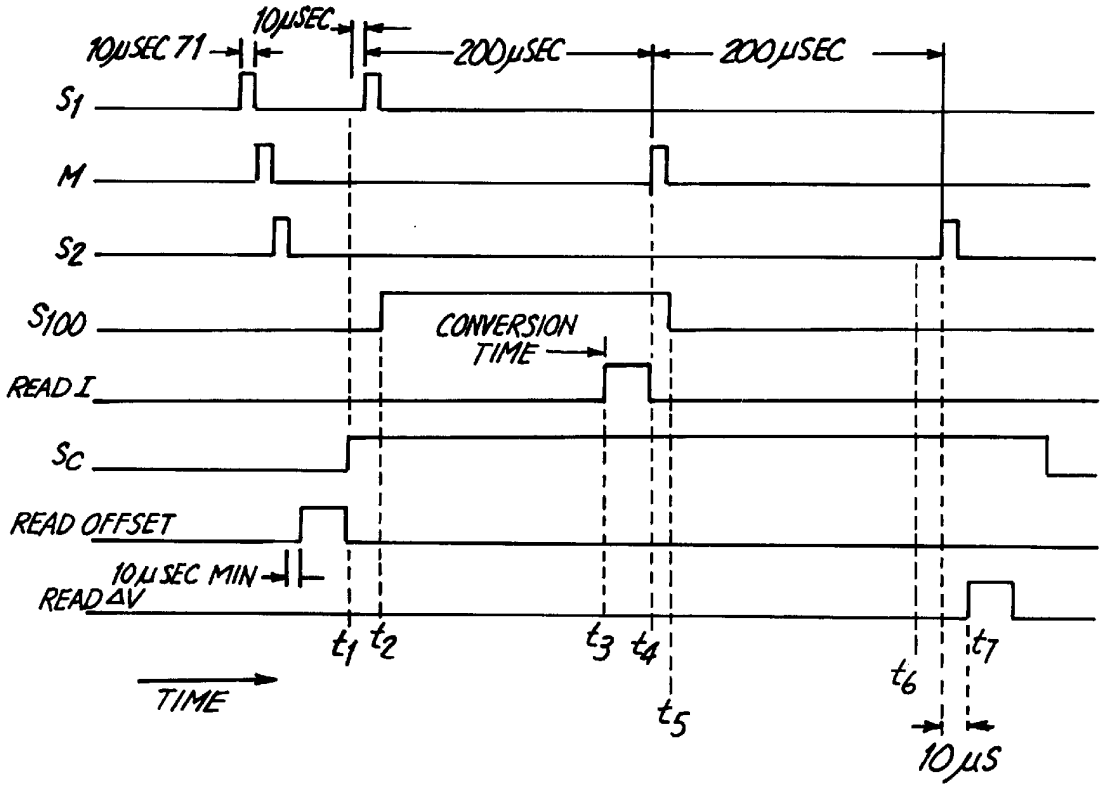
10μSEC
10μSEC 71
200μSEC
200μSEC
S1
M
S2
S100
CONVERSION TIME
READ I
SC
READ OFFSET
10μSEC MIN
READ ΔV
t1
t2
t3
t4
t5
t6
t7
10μS
TIME

Fig. 5

ELECTRONIC BATTERY TESTER

BACKGROUND OF THE INVENTION

This is a Divisional application of U.S. Ser. No. 09/006,226, filed Jan. 12, 1998, now U.S. Pat. No. 5,914,605 issued Jun. 22, 1999 which claims priority to Provisional Application Ser. No. 60/035,312, filed Jan. 13, 1997 and entitled "ELECTROINC BATTERY TESTER."

The present invention relates to battery testing devices. The present invention is particularly applicable to a technique for measuring conductance of a battery in which a small resistive load is momentarily placed across the battery and the change in voltage is monitored.

Chemical storage batteries, such as lead acid batteries used in automobiles, have existed for many years. In order to make optimum use of such a battery, it is very desirable to test the battery to determine various battery parameters such as state of charge, battery capacity, state of health, the existence of battery defects.

Various techniques have been used to measure battery parameters. For example, hygrometers have been used to measure the specific gravity of a battery and simple voltage measurements have been used to monitor the voltage of the battery. One battery testing technique which has been popular for many years is known as a load test in which a battery is heavily loaded over a period of time and the decay in the battery output is monitored. However, such a test is time consuming and leaves the battery in a relatively discharged condition. Further, such a tester must be made relatively large if it is to be used with large batteries.

A much more elegant technique has been pioneered by Midtronics, Inc. of Burr Ridge, Ill. and Dr. Keith S. Champlin in which battery parameters are determined based upon a measurement of the battery's conductance. This work is set forth in, for example, the following patents issued to Champlin: U.S. Pat. No. 3,873,911; U.S. Pat. No. 3,909,708; U.S. Pat. No. 4,816,768; U.S. Pat. No. 4,825,170; U.S. Pat. No. 4,881,038; U.S. Pat. No. 4,912,416; U.S. Pat. No. 5,140,269; U.S. Pat. No. 5,343,380; U.S. Pat. No. 5,572,136; and U.S. Pat. No. 5,585,728 and the following patents assigned to Midtronics, Inc., U.S. Pat. No. 5,574,355 and U.S. Pat. No. 5,592,093.

However, there is an ongoing need to refine battery testing techniques, improve their accuracy and improve the types of applications in which they may be successfully employed.

SUMMARY OF THE INVENTION

A microprocessor couples to a voltage sensor through an analog to digital converter. The voltage sensor is adapted to be coupled across terminals of a battery. A small current source is also provided and adapted to be coupled across the terminal to the battery. The current source is momentarily switched on to provide a current (which may be a current drop) through the battery and the resulting change in voltage is monitored using the microprocessor. The microprocessor calculates battery conductance based upon the magnitude of the current and the change in voltage. These techniques are employed to overcome noise from noise sources which may be coupled to the battery during the battery test.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a simplified electrical schematic diagram of a battery tester in accordance with the present invention.

FIG. **2** is a simplified electrical schematic diagram of a portion of sense circuitry shown in FIG. **1**.

FIG. **3** is a simplified electrical schematic diagram of a portion of sense circuitry shown in FIG. **1**.

FIG. **4** is a simplified electrical schematic diagram of a portion of sense circuitry shown in FIG. **1**.

FIG. **5** is a timing diagram showing various signals during operation of the circuitry of FIGS. **1** through **4**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIEMENTS

It has been discovered that measuring battery conductance of a storage battery connected to noise sources is a particularly difficult problem. Such noise sources include the charging system and various electronics in an automobile, for example, or other types of charging systems and electronics which may be connected to storage batteries. These noise sources interfere with the battery test. The present invention includes a number of techniques to overcome the limitations imposed by such noise.

FIG. **1** is simplified block diagram of a battery tester **10** in accordance with the present invention coupled to an electrical system **4**. Electrical system **4** is an model which includes a charge signal noise source **6** and a load signal noise source **8**. These sources could be, for example, the load and charger of an automobile or a uninterruptable power system (UPS).

Battery tester **10** determines the conductance of battery **12** in accordance with the present invention and includes test circuitry **16**. Circuitry **16** includes a current source **50** (which comprises, for example, a resistance R_L), sensor circuitry **52**, analog to digital converter **54** and microprocessor **56**. In one preferred embodiment, microprocessor **56** comprises a Motorola MC 68HC705C8P. Sensor circuitry **52** is capacitively coupled to battery **12** through capacitors C**1** and C**2** and has its outputs connected to a multiplexed or input of analog to digital converter **54**. A/D converter **54** is also connected to microprocessor **56** which connects to system clock **58**, memory **60**, output **62** and input **66**. Output **62** comprises, for example, a display and input **66** may comprise a keyboard, RF link, bar code reader, etc.

In operation, current source **50** is controlled by microprocessor **56** using switch **100** which may comprise, for example, a FET. Current source **50** provides a current I in the direction shown by the arrow in FIG. **1**. In one embodiment, this is a square wave or a pulse. The voltage sense circuitry **52** connects to terminals **22** and **24** of battery **12** to capacitors C**1** and C**2**, respectively, and provides an output related to the voltage difference between the terminals. Sense circuitry **52** preferably has a high input impedance. Note that circuitry **16** is connected to battery **12** through a four point connection technique known as a Kelvin connection. Because very little current flows through circuitry **52**, the voltage drop through its connections to battery **12** is relatively insignificant. The output of circuitry **52** is converted to a digital format and provided to microprocessor **56**. Microprocessor **56** operates at a frequency determined by system clock **58** and in accordance with program instructions stored in memory **60**.

In general, microprocessor **56** determines the conductance of battery **12** by actuating switch **100** to apply a current pulse with current source **50**. The microprocessor determines the change in battery voltage due to the current pulse using circuitry **52** and analog to digital converter **54**. The value of current I generated by current source **50** is measured by measuring the voltage drop across resistance R_L using amplifier **102**. Microprocessor **56** calculates the conductance of battery **12** as follows:

$$\text{Conductance} = G = \frac{\Delta I}{\Delta V} \quad \text{Equation 1}$$

where ΔI is the change in current flowing through battery **12** due to current source **50**, and ΔV is the change in battery voltage due to applied current ΔI. The relative conductance of battery **12**, as discussed with respect to FIG. **2**, is calculated using the equation:

$$\text{Relative Conductance}(\%) = \frac{G_{measured}}{G_{reference}} \times 100 \quad \text{Equation 2}$$

where $G_{measured}$ is the battery conductance in accordance with Equation 1 and $G_{reference}$ is a reference conductance value received through input **66** and stored in memory **60**. Generally, this reference conductance is determined based upon the type and characteristics of battery **12**. Microprocessor **56** can also operate using impedance measurements by inverting Equations 1 and 2. The relative conductance measurement may then be output using data output **62** which may comprise, for example, a display, meter, data link, etc.

The measurement of conductance in a noisy environment using circuitry **16** may be accomplished by maintaining a relatively short connection of resistance R_L across battery **12** and measuring the resultant small voltage drop. The DC voltage drop across the battery is a minimum of 2 volts and the absolute voltage drop across the battery may be any value. Sense circuitry **52** preferably has a relatively large gain which is saturated if circuitry **52** is directly coupled to battery **12**. Therefore, capacitors C**1** and C**2** are provided to capacitively coupled circuitry **52** to battery **12**.

FIG. **2** is a simplified electrical schematic diagram **110** of a portion of sense circuitry **52** shown in FIG. **1**. Circuitry **100** includes differential amplifier **112** having an inverting input connected to terminal **22** of battery **12** through capacitor C**1** and resistors **114** and **116** having values of 10 KΩ and 40.2 KΩ. The non-inverting input of amplifier **112** connects to terminal **24** through capacitor C**2** and resistors **118** and **120** having values of 10 KΩ and 40.2 KΩ, respectively. The non-inverting input of amplifier **112** connects to electrical ground through resistor **122** having a value of 1 MΩ feedback is provided from the output of amplifier **112** through resistor **124** having a value of 1 MΩ. Capacitors C**1** and C**2** have values of 0.1 μF and are ground through resistors **126** and **128** which have a value of 1 MΩ. Low impedance path resistors **130** and **132** have values of 1 KΩ and are selectively coupled to capacitors C**1** and C**2** through switches **134** and **136**, respectively. Switches **134** and **136** may comprise, for example, FETs which are controlled by microprocessor **56**.

In order to make accurate AC transient measurements, it is necessary that the bias voltage across the input coupling capacitors C**1** and C**2** remains relatively constant. This is facilitated by using relatively large capacitor values for C**1** and C**2** and employing coupled to a high input impedance circuit for circuit **52**. However, a significant drawback to the high impedance is that a relatively long time is required for the amplifier to stabilize to a quiescent operating point when the tester is first started or relocated to a different battery. Resistors **130** and **132** provide a relatively low impedance path to electrical ground when switches **134** and **136**, respectively, are actuated by microprocessor **56**. Preferably, the switches **134** and **136** are actuated just prior to measurements to thereby quickly establish the operating point of the system. A further advantage of application of the low impedance paths during a non-test interval is that they allow quiescent operating points that are elevated (or depressed) due to system noise, thereby placing no practical limit on the amount of low frequency noise that can be rejected.

Another source of inaccuracy due to noise in the system is the variability in the voltage bias at the inputs of capacitors C**1** and C**2** which arises due to the inductive coupling of the pulse generated by source **50** to the voltage sense leads which couple circuitry **52** to battery **12**. This causes relatively large voltage spikes in the connection leads which could damage the sense circuitry leading to inaccurate readings. Diode pairs **152** and **154** are provided as input protection devices to eliminate this and exasterbate this problem by tying one side of capacitor C**1** and C**2** to a power supply rail through an extremely low impedance path (the forward diode direction). In order to overcome this problem, switches **160** and **162** are provided which selectively as shown in FIG. **3** couple capacitors C**1** and C**2** to resistors **114** and **118**, respectively. Switches **160** and **162** may comprise, for example, FETs which are controlled by microprocessor **56**. Microprocessor **56** controls switches **160** and **162** to provide an open circuit during the occurrence of any voltage that exceeds the value of the power supply rails. Leakage is only about 1 nanoamp. This allows capacitors C**1** and C**2** to "free wheel" during a voltage spike with no resultant in charging.

Another aspect of the invention includes the determination of the quiescent operating point of the battery voltage during application of the current pulse from source **50**. It is desirable to exactly determine this applicating point. However, this is not possible because the current pulse has changed the operating point by an amount inversely proportional to the conductance. Additionally, the quiescent point varies according to the AC or DC noise which is present on the system. The present invention estimates the quiescent operating point during the current pulse by taking samples before and after the current pulse and averaging the difference. FIG. **4** is a simplified electrical schematic diagram of circuitry **180** which is part of circuitry **52** shown in FIG. **1**. Circuitry **180** includes circuitry **52** as shown in FIG. **1**. Circuitry **180** includes three sample and hold elements **182**, **184** and **186** which couples to amplifier **112** shown in FIGS. **2** and **3**. Additionally, sample and hold circuits **182** through **186** receive control signals S_1, M, and S_2 from microprocessor **56**. The output from amplifier **102** is also shown connected to analog to digital converter **54**. Analog to digital converter **54** includes a multiplex input which is controlled by MUX line from microprocessor **56** to select one of the inputs from amplifier **102** or sample and-hold circuits **182** through **186**.

FIG. **5** is a timing diagram showing operation of the circuitry in FIGS. **1** through **4**. Signal S_1 is applied by microprocessor **56** to sample and hold circuit **182**, signal M is applied to sample and hold circuit **184** and signal S_2 is applied to circuit **186** shown in FIG. **4**. Signal S_{100} controls switch **100** shown in FIG. **1**. The READ I signal couples analog to digital converter **54** to amplifier **102** to thereby read the voltage drop across resistance R_L. The S_C signal controls switches **160** and **162** shown in FIG. **3**. The READ OFFSET signal controls analog to digital converter **54** to initially read offsets from sample and hold **182** through **186**. The read ΔV signal controls reading of the sample and hold circuits **182** through **186** with the A/D **54** following a measurement cycle. During operation, the values of the three sample and holds are initially latched using the first pulse shown in signals S_1, M, and S_2. During this initial reading, switches **160** and **162** are open such that the voltages V^0_{S1},

V^{O}_{M}, V^{O}_{S2} present on these latches constitute offset values. These offsets are stored in memory **60** and subtracted from subsequent voltage measurements by microprocessor **56** to thereby reduce errors. At time t_1 switches **160** and **162** are closed by signal S_C and sample and hold circuit **182** is again latched using signal S_1 to store the first measured voltage V_1. At time t_2, current I is applied to battery **12** by closing switch **100** with signal S_{100}. After about 150 μS, the READ I is used to control A/D converter **54** to read the voltage output from amplifier **102**. At time t_4, sample and hold circuit **184** is triggered by signal M to store the current voltage V_M across battery **12**. At time t_5, the current I is removed from battery **12** and after a settling period of approximately 200 μS, sample and hold circuit **186** is triggered by signal S2 to store V_2. At time t_7, the A/D converter **54** to convert the voltage difference of the sample stored in circuits **182** and **186**. In various embodiments, this difference may be determined using analog subtraction techniques or digital subtraction using microprocessor **56**. The change in voltage of the battery due to applied current I is then calculated using the formula:

$$\Delta V = \frac{[(V_1 - V_1^0) + (V_2 - V_2^0)]}{2} - (V_M - V_M^0) \qquad \text{Equation 3}$$

G is then determined using the formula:

$$G = \frac{(V_M - V_M^0)/R_L}{\Delta V} \qquad \text{Equation 4}$$

As can be seen in Equations 3 and 4, the offset values V^{O}_{1}, V^{O}_{2} and V^{O}_{M} are subtracted from the measured values to thereby remove any systems offsets.

Another source of errors in measurement in noisy environments is due to lumped sum non-linearities in the circuit. In general, the equation for conductance is G=I/V, where G represents the conductance in mhos, I represents the current differential in amps and V represents the voltage differential in volts. Non-linearities in circuit **16** may cause a small offset component in the measured value of V. This offset may be determined during manufacture or during later calibration of circuitry **16** by forcing the input to circuitry **16** to 0 volts and measuring the resultant voltage. This voltage value (X) is stored in memory **60** and used to modify the equation for conductance by subtracting the offset from all measurements G=I/(V−X).

In another aspect of the invention, non-linearities in circuitry **16** are compensated or "linearized" using a second order polynomial equation. Such non-linearities may be due to many factors including cabling, PCB layout, magnetic effects, etc. The polynomial is determined by measuring a plurality of calibrated standards using an uncalibrated tester **16** and the resultant data is fit to a curve using curve fitting techniques. For example, Table 1 is a series of measurements of seven different test cells having known voltage and conductance values by a battery tester prior to such calibration:

TABLE 1

CELL	VOLTS	MEASURED MHOS	ACTUAL MHOS	% ERROR
1	4.40	648	800.73	+23.57
2	4.40	1080	1333.33	+23.46
3	4.42	1638	2000.16	+22.11
4	4.42	2194	2665.10	+21.47
5	4.42	3341	4000.00	+19.72
6	4.44	5107	6001.68	+17.52
7	4.44	6968	7995.52	+14.75

Using a least squares curve fitting technique, a quadratic equation of the form:

$$G_{actual} = 1{,}34894810^{-1} + 1.245607 G_{measured} - 1.40414210^{-5} G^2_{measured} \qquad \text{Equation 5}$$

Equation 5 can be used to calibrate the measured value of mhos. The three constants in Equation 5 are stored in memory **60** for use by microprocessor **56**.

Another technique of the present invention to overcome problems associated with noise includes employing statistical algorithms in microprocessor **56**. Amplifier **12** is instantly able to take readings at any point, regardless of prior disturbance of the quiescent operating point due to noise, in other words, quiescent disturbances do not require a long "settling period" following the disturbance before another reading can be taken. If the noise signal remains linear and continuous, readings can be taken during the noise signal itself. However, difficulties arise in very high noise environments, where the noise is of large value, and not linear or continuous (for example, UPS switching currents). This "impulse" noise present during the measurement period causes incorrect values to be recorded for that sample, even though they do not affect the ability of the amplifier to take another sample immediately following it. Noise pulses of particular concern are high amplitude, short duration, low frequency (360 Hz, for example) spikes. Since the measurement period is short (200 micro-seconds), circuit **16** can take a large number of measurements in a short period of time. In doing so, there is a high incidence of samples containing the correct value of conductance, and a lower number of samples containing corrupted data. Microprocessor **56** determines the median or mean values over a large number of samples and is thereby able to intelligently decode the correct value from the scattered measured data.

Although the present invention has been described with reference to preferred embodiments, workers skilled in the art will recognize that changes may be made in form and detail without departing from the spirit and scope of the invention.

What is claimed is:

1. An apparatus for measuring condition of a storage battery, comprising:

a first connector adapted to connect to a positive terminal of the storage battery;

a second connector adapted to connect to a negative terminal of the battery;

an analog to digital converter coupled to the first and second connectors adapted to amplify a signal from the battery developed between the positive terminal of the battery and the negative terminal of the battery and responsively provide a digital output;

a memory storing a calibration value, the calibration value related to lumped sum non-linearities in the apparatus; and

a microprocessor coupled to the analog to digital converter adapted to measure condition of the storage

battery in response to the digital output, and wherein the measurement is a function of the calibration value whereby the calibration value is used to reduce offsets in the measurement due to lumped sum non-linearities.

2. The apparatus of claim **1** wherein the calibration value comprises a voltage value and the condition of the battery is a function of battery conductance.

3. The apparatus of claim **1** wherein the first and second connectors comprise Kelvin connections.

4. The apparatus of claim **1** wherein the calibration value is determined by measuring an offset in the digital output.

5. The apparatus of claim **4** wherein the calibration value is determined during manufacture.

6. The apparatus of claim **1** wherein the signal from the battery is developed in response to an applied current.

7. The apparatus of claim **1** wherein the signal from the battery is developed in response to an applied voltage.

8. The apparatus of claim **1** wherein the signal from the battery is developed in response to an applied load.

9. A method of measuring condition of a storage battery, comprising:

applying a signal to the storage battery;

sensing a response signal from the storage battery generated in response to the applied signal;

digitizing the response signal;

retrieving a calibration value from a memory, the calibration value related to lumped sum non-linearities of battery test circuitry; and

determining condition of the battery as a function of the response signal and the calibration value whereby the calibration value is used to reduce offsets in the measurement due to lumped sum non-linearities.

10. The method of claim **9** wherein the applied signal is a current.

11. The method of claim **9** wherein the applied signal is a voltage.

12. The method of claim **9** wherein the applied signal is a load.

13. The method of claim **9** wherein the calibration value is determined by measuring an offset in the digital output.

14. The method of claim **13** wherein the calibration value is determined during manufacture.

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